AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A client-server semiconductor verification system, said system comprising:

a client ~~device~~ computer storing a test job for testing a design of a programmable logic circuit, said test job having test vectors and configuration data for said programmable logic circuit;

a server coupled to said client ~~device~~ computer by way of a network, said server receiving said test job from said client ~~device~~ computer; and

a system under test coupled to said server and having said programmable logic circuit which is configured with a circuit design implemented according to ~~using~~ said configuration data, said system under test receiving said test vectors and outputting result vectors to the client ~~device~~ computer by way of said server.

2. (Currently Amended) The system of claim 1 wherein said client ~~device~~ computer further has expected results.

3. (Currently Amended) The system of claim 2 wherein said client ~~device~~ computer generates said test vectors.

4. (Currently Amended) The system of claim 3 wherein said client ~~device~~ computer generates said expected results.

5. (Original) The system of claim 2 wherein said test vectors and said expected results are generated by an external device.

6. (Currently Amended) A client-server semiconductor verification system, said system comprising:

a plurality of client ~~devices~~ computers, wherein a client ~~device~~ computer

of said plurality generates a test job for testing the design of a programmable logic circuit and comprises test vectors and configuration data for said programmable logic circuit;

a server coupled to said plurality of client ~~devices~~ computers by way of a network, said server receiving said test job from said client ~~device~~ computer; and

a system under test coupled to said server, said system under test having said programmable logic circuit which is configured with a circuit design implemented according to said configuration data and receiving said test vectors and outputting result vectors to the client ~~device~~ computer by way of the server.

7. (Original) The system of claim 6 wherein said server comprises a network interface.

8. (Original) The system of claim 6 wherein said server comprises a system under test interface.

9. (Original) The system of claim 6 further comprising a plurality of systems under test.

10. (Currently Amended) The system of claim 6 further comprising another server coupled to said plurality of client ~~devices~~ computers by way of the network.

11. (Currently Amended) A client-server semiconductor verification system, said system comprising:

a plurality of client ~~devices~~ computers, wherein a client ~~device~~ computer of said plurality ~~generating~~ generates a test job for testing the design of a programmable logic circuit and ~~having~~ has test vectors and configuration data for said programmable logic circuit;

a job distribution server coupled to said plurality of client ~~devices~~ computers by way of a network, said job distribution server receiving said test job from said client ~~device~~ computer;

a server coupled to said plurality of client ~~devices~~ computers by way of said job distribution server, said server receiving said test job from said job distribution server; and

a system under test having programmable logic which is configured with a circuit according to said configuration data of said test job coupled to said system under test and being coupled to said server, said system under test receiving said test vectors and outputting result vectors to said client ~~device~~ computer by way of said server and said job distribution server.

12. (Currently Amended) The system of claim 11 further comprising a plurality of servers coupled to said plurality of client ~~devices~~ computers by way of said job distribution server.

13. (Original) The system of claim 12 wherein said plurality of servers are coupled to said job distribution server by way of a second network.

14. (Original) The system of claim 11 further comprising a plurality of systems under test.

15. (Currently Amended) The system of claim [[11]] 14 wherein each system under test of said plurality of systems under test is coupled to a server of said plurality of servers.

16. (Currently Amended) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

storing a test job for testing a design of a circuit in a client ~~device~~ computer, said test job having test vectors and configuration data for a circuit implemented in programmable logic;

configuring a system under test having said circuit implemented in said programmable logic with a circuit design according to said configuration data of said test job by way of [[said]] a test server;

coupling said test vectors to said system under test;

receiving an output comprising result vectors from said system under test; and

comparing said result vectors from said system under,test to expected result vectors.

17. (Currently Amended) The method of claim 16 further comprising a step of generating said test vectors at said client ~~device~~ computer.

18. (Original) The method of claim 16 further comprising a step of generating said test vectors and expected result vectors on an external device.

19. (Original) The method of claim 16 wherein said step of coupling said test vectors to a system under test comprises coupling test vectors by way of a test server.

20. (Currently Amended) The method of claim 19 further comprising a step of coupling said result vectors to said client ~~device~~ computer by way of said test server.

21. (Currently Amended) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client ~~devices~~ computers to a test server, each said client ~~device~~ computer storing a test job for testing the design of a programmable logic circuit, said test job having test vectors and configuration data for said programmable logic circuit;

reconfiguring a programmable logic circuit of a system under test with a circuit design according to said configuration data of said test job by way of said test server;

coupling test vectors of a predetermined test job to said system under test by way of said test server;

receiving an output comprising result vectors from said system under

test; and

comparing said result vectors from said system under test to expected result vectors.

22. (Original) The method of claim 21 further comprising a step of coupling a plurality of systems under test to said test server.

23. (Original) The method of claim 21 further comprising a step of providing a test server having a network interface and a system under test interface.

24. (Currently Amended) The method of claim 23 further comprising a step of coupling said result vectors to said client ~~device~~ computer by way of said test server.

25. (Currently Amended) The method of claim 21 wherein said step of comparing said result vectors from said system under test to expected result vectors comprises comparing said result vectors from said system under test to expected result vectors at said client ~~device~~ computer.

26. (Currently Amended) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client ~~devices~~ computers to a job distribution server, each said client ~~device~~ computer storing a test job for testing the design of a programmable logic circuit and having test vectors and configuration data for said programmable logic circuit;

reconfiguring a programmable logic circuit of a system under test with a circuit design according to said configuration data of said test job by way of said test server;

coupling said job distribution server to a plurality of servers, each said server coupling predetermined test vectors to a system under test of a plurality of systems under test;

receiving an output comprising result vectors from a system under test of said plurality of systems under test; and

comparing said result vectors from said system under test to expected result vectors.

27. (Currently Amended) The method of claim 26 further comprising a step of providing a first network between said plurality of client ~~devices~~ computers and said job distribution server.

28. (Original) The method of claim 27 further comprising a step of providing a second network between said plurality of servers and said job distribution server.

29. (Original) The method of claim 26 further comprising coupling a plurality of systems under test to a server of said plurality of servers.

30. (Currently Amended) The method of claim 26 further comprising a step of coupling said output comprising result vectors to a client computer.